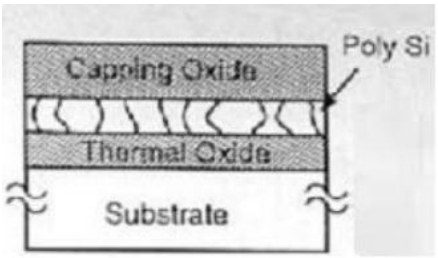
Silicon on Insulator

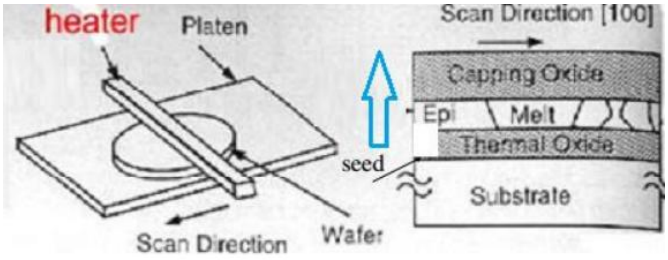
I. Introduction

- **Definition**
  - Silicon on insulator (SOI) technology refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates in semiconductor.
- **Benefits**
  - Reduce parasitic capacitance.
  - Immune to Latch-up problem
- **Problems**
  - Increase in substrate cost.
  - Lattice mismatch
- **Process "Silicon on Sapphire (SOS)"**
  - First CVD of Si using SiH_4 then annealing.
  - Si/Al_2O_3 interface is moderate quality (lattice mismatch).
  - Deep implant of Si^+ to improve the interface.
  - Second CVD and annealing to increase Silicon and to crystallize.

II. Zone-Melting Recrystallization

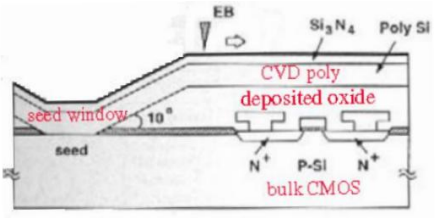
- ZMR technology produces SOI structures by recrystallization of poly-silicon films, deposited on oxidized silicon wafers.
- Steps:
  - Thermal oxide growth (1-2 mm thick), acts as BOX layer.
  - Etch oxide at the edge of wafer to expose a Silicon seed (substrate).
  - Poly-silicon is deposited by LPCVD (0.5-1.0 mm thick)
  - A capping oxide is thermally deposited (2 mm thick) as a protection against oxidation.
  - Graphite rod heater scans the wafer slowly (0.1 mm/s).
  - Recrystallization starts at the exposed seed (bottom-up).
  - As a result, full liquid recrystallization of silicon wafer can be carried out and poly-silicon turns into high-quality Silicon.
  - The predominant defects that limit the wide application of ZMR SOI materials are grain sub-boundaries.





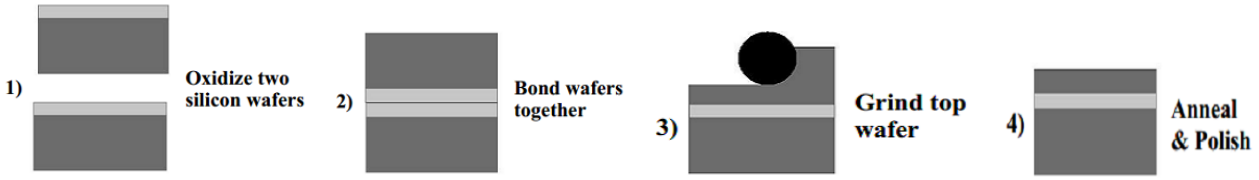
III. Epitaxial lateral overgrowth

- Using Electron beam for forming the above silicon layer through the seed.
- Used in integration 3-D stacked circuits.
- Steps:
  - Build bulk CMOS
  - Deposit oxide
  - Open seed window
  - Deposit poly, nitride (nitride=capping layer to protect against oxidation during EB scan)
  - EB scan for ELO
  - Build the upper SOI CMOS



IV. Wafer Bonding

- Start by 2 wafers (Device & Support).
- Thermally oxide both wafers.
- Bond the 2 oxides by pressing in an oxidizing ambient at 700 C.
- Top wafer is thinned by grinding.
- Anneal & Polish.



V. SIMOX "Separation by Implantation of Oxygen"

- It is an SOI fabrication technology.
- Implant a layer of oxygen by ion Implantation.
- High temperature anneal to form the buried insulating layer.

VI. ITOX "Internal Thermal Oxidation"

- It is an improvement for SIMOX technology.
- High temperature oxidation step after SIMOX process results in surface and internal oxide.
- Make the surface oxide thinner.
- Etch the upper oxide.

VII. Unibond (Smart-Cut)

- Use 2 oxidized wafers A and B
- Implant H+ in wafer A under the oxide at a depth = active Si film.
  - Implanted H atoms gather to form micro-cavities.
  - The wafers separate upon heating if sufficient H atoms were implanted.
- Bond wafers A and B
- Heat at 400-600oC to separate the bonded wafers at the implanted H level (smart-cut).